REMARKS

Claims 1-26 were examined and reported in the Office Action. Claims 1-26 are rejected. Claims 1, 10, 19 and 23 are amended. Claims 1-26 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103(a)

A. It is asserted in the Office Action that claims 1-18 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 5,467,473 issued to Kahle ("Kahle") in view of *On the Value Locality of Store Instructions*, Lepak, K.M, Lipasti, M.H., Computer Architecture, 2000, Proceedings of the International Symposium on June 10-14, 2000 ("Lipasti") and further in view of U.S. Patent No. 5,987,595 issued to Yoaz ("Yoaz"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be*

considered in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 1 contains the limitations of

> a predictor having a collision history table (CHT), said predictor for predicting silent store instructions; a processing section coupled to the predictor, the processing section including an extended load buffer coupled to the predictor; a marking processing section; a comparing processing section; and a recovery processing section, wherein unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions, wherein the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

Applicant's claim 10 contains the limitations of

> a processor having internal memory, a bus coupled to the processor; a memory coupled to a memory controller and the processor; wherein the processor includes: a predictor having a collision history table (CHT), said predictor for predicting silent store instructions; an extended load buffer coupled to the predictor; a marking process; a comparing process; and a recovery process, wherein unexecuted load instructions are advanced over associated store instructions without flushing the load instructions, and the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

Kahle discloses a comparison technique for reordering load and store instructions, which were executed out of order. It is asserted in the Office Action that Kahle does not disclose "a silent store instruction or advancing dependent loads ahead

of silent stores the loads were dependent upon. (Office Action, page 3, section 5). At column 2, lines 56-59, Kahle discloses that "[d]uring execution of the store instruction, the address is compared to the address of *previously executed load instructions*, in a load queue, which executed out of order ahead of the store." Therefore, Kahle does not teach, disclose or suggest "the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction." Further, Kahle does not teach, disclose or suggest " a recovery processing section, wherein unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions."

It is asserted on page 5 of the Office Action, paragraph that Lipasti discloses the notion of a silent store (referring to Lipasti, page 183, column 2, last paragraph). Lipasti, however, is not asserting a silent store predictor where silent stores are tracked and unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions. Lipasti's section 2.0 refers to understanding of the value locality of store data values. The stride predictor that is referenced in the Office Action is used for the results listed in Table I, which are store value locality measurements for various benchmarks, and have nothing to do with silent store prediction. Lipasti does not teach, disclose or suggest silent store prediction. Moreover, Lipasti does not teach, disclose or suggest

> a recovery processing section, wherein unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions, wherein the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

Applicant notes the assertion in the Office Action that motivation to combine the teachings of Lapasti is for "improving memory performance of the memory access path, and allowing a designer to obtain greater performance from existing structures or reduction in size and complexity of the system." These goals for improvements, however, are goals that every designer has. That is, every designer must be motivated to improve performance, otherwise there is no point in designing. Therefore, Applicant fails to see proper motivation for a combination.

Yoaz is a same inventor of the presently claimed Application. Yoaz discloses a load predictor for predicting where a load instruction will collide, and determining how far the load instruction can be advanced without leading to a collision. Yoaz also discloses a collision history table (CHT). Yoaz, however, does not teach, disclose or suggest a predictor for predicting silent stores, nor does Yoaz teach, disclose or suggest

> a recovery processing section, wherein unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions, wherein the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

According to MPEP 2142,

> [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of

> the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to silent store prediction, as disclosed, in order to improve performance and power from, e.g., better memory disambiguation or reduced cache/memory traffic. Further, no thought would have been made regarding

> a recovery processing section, wherein unexecuted load instructions are advanced over associated silent store instructions without flushing the load instructions, wherein the predictor compares an unexecuted load instruction value with an issued and unexecuted store instruction value, and the unexecuted load instruction bypasses the issued store instruction for execution if the unexecuted load instruction value and the issued and unexecuted store value are the same, and the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

Since neither Kahle, Yoaz, Lipasti, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's claims 1 and 10, as listed above, a resulting combination would still not render Applicant's claimed invention. And, since neither Kahle, Yoaz, Lipasti, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's claims 1 and 10, as listed above, Applicant's claims 1 and 10 are not obvious over Kahle in view of Yoaz and further view of Lipasti since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 1 and 10, namely claims 2-9, and 11-18, respectively, would also not be obvious over Kahle in view of Yoaz and further in view of Lipasti for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 1-18 are respectfully requested.

B. It is asserted in the Office Action that claims 19-20, 22-24, 26 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Kahle in view of Lipasti. Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's claim 19 contains the limitations of

> fetching an instruction and determining if an instruction is one of a store and a load; performing a silent store prediction if the instruction is a store; issuing the store instruction; comparing an address and data of the store instruction with load instructions in an extended load buffer; setting marking bits in the extended load buffer if a match is found in the comparing; updating a memory with the store instruction if the store instruction can be retired; and bypassing a predicted silent store instruction if an associated unexecuted load instruction value matches the issued and unexecuted store instruction value and executing the load instruction ahead of the predicted silent store instruction without flushing load instructions, wherein the unexecuted load instruction is dependent on the issued and unexecuted store instruction.

Applicant's claim 23 contains the limitations of

> fetch an operation and determining if the operation is one of a store instruction and a load instruction; perform a silent store prediction if the operation is a store instruction; execute the store operation; compare an address and data of the store operation with load operations in an extended load buffer; set marking bits in the extended load buffer if a match is found in the compare instruction; update a memory with a store operation if the store operation can be retired; and bypass a predicted silent store operation and execute an associated load operation ahead of the silent store operation without flushing load instructions if the operation is a load and the load operation includes a value that matches a value included in the store operation, wherein the load operation is unexecuted and is dependent on the silent store operation.

Similarly with regard to claims 1 and 10 addressing Kahle and Lipasti above in section I(A), neither Kahle nor Lipasti teach, disclose or suggest the limitations contained in amended claim 19 of

> performing a silent store prediction if the instruction is a store;... setting marking bits in the extended load buffer if a match is found in the comparing; updating a memory with the store instruction if the store instruction can be retired; and <u>bypassing a predicted silent store instruction if an associated unexecuted load instruction value matches the</u>

> issued and unexecuted store instruction value and executing the load instruction ahead of the predicted silent store instruction without flushing load instructions, wherein the unexecuted load instruction is dependent on the issued and unexecuted store instruction

or the limitations contained in amended claim 23 of

> perform a silent store prediction if the operation is a store instruction; execute the store operation; ... set marking bits in the extended load buffer if a match is found in the compare instruction; update a memory with a store operation if the store operation can be retired; and bypass a predicted silent store operation and execute an associated load operation ahead of the silent store operation without flushing load instructions if the operation is a load and the load operation includes a value that matches a value included in the store operation, wherein the load operation is unexecuted and is dependent on the silent store operation.

Since neither Kahle, Lipasti, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's claims 19 and 23, as listed above, a resulting combination would still not render Applicant's claimed invention. And, since neither Kahle, Lipasti, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's claims 19 and 23, as listed above, Applicant's claims 19 and 23 are not obvious over Kahle in view of Lipasti since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 19 and 23, namely claims 20 and 22, and 24 and 26, respectively, would also not be obvious over Kahle in view of Lipasti for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 19-20, 22-24, 26 are respectfully requested.

C. It is asserted in the Office Action that claims 21 and 25 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Kahle in view of Lipasti as applied to claims 19-20, 22-24, and 26 above, and further in view of Yoaz. Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant's claim 21 directly depends on amended claim 19. Applicant's claim 25 directly depends on amended claim 23.

Similarly to the discussion above in sections I(A-B), neither Kahle, Lipasti, Yoaz, nor the combination of the three, teach, disclose or suggest

> bypassing a predicted silent store instruction if an associated unexecuted load instruction value matches the issued and unexecuted store instruction value and executing the load instruction ahead of the predicted silent store instruction without flushing load instructions, wherein the unexecuted load instruction is dependent on the issued and unexecuted store instruction

nor

> bypass a predicted silent store operation and execute an associated load operation ahead of the silent store operation without flushing load instructions if the operation is a load and the load operation includes a value that matches a value included in the store operation, wherein the load operation is unexecuted and is dependent on the silent store operation.

Since neither Kahle, Lipasti, Yoaz, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's claims 19 and 23, as listed above, a resulting combination would still not render Applicant's claimed invention. And, since neither Kahle, Lipasti, Yoaz, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's claims 19 and 23, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claims 19 and 23 are not obvious over Kahle in view of Lipasti, in further view of Yoaz since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 19 and 23, namely claims 21, and 25, respectively, would also not be obvious over Kahle in view of Lipasti in further view of Yoaz for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 21 and 25 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-26 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: July 19, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on July 19, 2005.

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Jean Svoboda